IN THE SPECIFICATION:

Please replace paragraph **[0008]** with the following replacement paragraph:

[0008] The gate driver 8 sequentially supplies the gate high voltage signal to the gate lines (G1 to Gn ~~GN~~) according to a gate start pulse signal (GSP) received from the timing controller 4. Accordingly, the gate driver 8 includes a plurality of gate drive integrated circuits (not shown), commonly referred to as gate driving ICs, for separately and sequentially driving the gate lines (G1 to Gn). Each of the gate driving ICs include a shift register responding to the gate start pulse signal (GSP) and a gate shift clock signal (GSC) provided from the timing controller 4. In addition, the gate driving ICs sequentially generate a gate high voltage signal and include a level shifter for shifting voltages of the gate high voltage signal to suitable levels for driving the thin film transistor. When the gate start pulse signal (GSP) is supplied from the timing controller 4, the gate driving ICs respond to the gate shift clock signal (GSC) and sequentially supplies the gate high voltage signal having one horizontal period (1H) to the gate lines (G1 to Gn) by performing a shift operation.

Please replace paragraph **[0026]** with the following replacement paragraph:

[0026] ~~FIGs. 8A~~ FIGs. 8A and 8B are diagrams showing flicker inspection patterns of a 2-dot inversion system according to the related art. In FIG. 8A, during the 2-dot inversion driving method, a flicker inspection pattern (i.e., the first flicker inspection pattern) shows that the

polarity of data supplied to the liquid crystal display panel is changed by a 1-dot unit along a horizontal direction and is changed by a 2-dot unit along a vertical direction and is supplied as a half-gray pattern to a green sub-pixel of the negative polarity (-), and a black pattern to red and blue sub-pixels. Accordingly, if the first flicker inspection pattern is displayed on the liquid crystal display panel driven using the 2-dot inversion method, the flicker can be adjusted since components of a ½-frame frequency, i.e., frame frequency divided in half, appear due to the half-gray pattern of the negative polarity (-).

Please replace paragraph **[0074]** with the following replacement paragraph:

[0074] The first polarity inversion signal generator 102 may include a second D flip-flop ~~102afor~~ 102a for executing one frequency division to produce the polarity signal (POLS) received from the polarity signal generator 100. Accordingly, the second D flip-flop 102a may receive the polarity signal (POLS) as a clock signal, may execute a one frequency division, and may supply polarity signal (POLS) to the first polarity inversion signal selector 104.

Please replace paragraph **[0077]** with the following replacement paragraph:

[0077] The first polarity inversion signal selector 104 selects, in accordance with the selection signal from the first selection signal generator 110, any one of the non-inverted first polarity inversion signal (POL1) and the inverted first polarity signal (POL1) received respectively from

the non-inversion output terminal (Q2) and the inversion output terminal (BG2) of the first polarity inversion signal generator 102. Accordingly, the first polarity inversion signal selector 104 may include a multiplexer having two inputs and one output. The multiplexer 104 may be connected to the first selection signal generator 110, i.e., a third D flip-flop 100a, that may generate a selection signal (CS) (not shown) inverted for each frame. The third D flip-flop 110a may receive the feedback signal from its inverted output terminal (BQ3), synchronize the feedback signal with a rising edge of an inverted vertical synchronization signal (Vsync), and generate the selection signal (CS). Accordingly, the selection signal (CS) generated may be supplied to the input terminal of the first polarity inversion signal selector 104 through non-inverted output terminal (Q3). Since the selection signal (CS) is generated at a reference of the vertical synchronization signal (Vsync), the selection signal (CS) may be inverted on a frame-by-frame basis. Thus, the ~~miltiplexer~~ multiplexer 104 may generate the first polarity inversion signal (POL1) due to the selection signal (CS) received from the third D flip-flop 110a inverted on a frame-by-frame basis, and supply the inverted signal to the second polarity inversion signal generator 106, and to the polarity inversion signal output part 108.